Robustness analysis in SRAM bit cells

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***Abstract*—This work evaluates the main characteristics related to SRAM cells. Five SRAM topologies cells are evaluated: the 8T, 9T, 8TSER, DICE and the traditional 6T. The analysis explores cell delay times, energy consumption, noise tolerance and the impact of radiation-induced transient faults. All cells adopts the 16nm bulk CMOS technology. The 8T cell presents the the lowest energy consumption, 22% less than 6T power consumption. The 8TSER is the most tolerant cell to static noise, 3x more than 6T. The DICE cell is the most robust choice for radiation effects, 10x more robust than 6T.**

***Index Terms*—SRAM, Reliability, Soft Erros, Single Event Upset, Noise, Delay Times.**

I. Introduction

Static Random-Access Memory (SRAM) is a critical component within integrated circuits. The main characteristics considered on the SRAM cell choice in a design are the access speed during the operations, the stability in retaining stored data, and, the ability to work at low voltages, mainly on the SRAM design for high performance applications [1]. Historically, SRAM has been used through cache levels, where memory cells are designed in the same processor technology node. Cache memory design significantly influences total system performance. Factors such as footprint, runtime and power optimization are impacted by SRAM structure [2].

The growing demand for performance in contemporary applications impact on the need for more memory. Currently, SRAMs occupy the largest block of area in a computer system, about 70% of the System Area on Chip (SoC) [3] and 90% of the Processor Area [4]. With the technology scaling, the area has no longer been a significant problem, allowing a large integration scale of cache levels inside the processors chip.

The reduction in the sizing scales, the increase the operating frequency and the reduction the supply voltage, this cause an increase in the susceptibility of faults due to interactions with the external environment. The most common events are static noise and especially the collision of radiation particles particles [5] . When a data or logical value is changed as a result of this interaction with the environment and has a temporary effect, this event is called a transient fault or Soft Error [6]. In this type of event, after a certain period of time, the behavior of the circuit returns to normal.

Transient faults derived from the radiation effects, happen when an energised particle strike a susceptible node of the transistor. This particle deposits charge in this region and may create a conduction channel between the PN junction of a reverse polarized transistor [7]. In a SRAM circuit, this event can reflect in a change in the value stored by the cell. When this occurs, the affected node is characterized as a sensitive or critical node. In the past, these transient effects due to radiation were observed only in space environments and/or hostile to radiation. Nowadays, they are a reality even at the terrestrial level [7] [8].

Five SRAM cell topologies were explored: SRAM 8T which has a dedicated mechanism that isolates the internal nodes during reading operations [9]. SRAM 9T, which is based on 8T and proposes improvements for leakage current problems [9]. SRAM DICE, a well-known Single Event Upset robust cell topology, which uses a redundancy mechanism between its internal nodes [10]. SRAM 8T-SER, which is a proposal of Soft Error robust cell in general, does not have dedicated reading mechanisms and is compatible with low voltage operations [11]. Besides, of course, the conventional SRAM 6T cell, the most used in the industry and documented in the literature [12]. The electric diagram of all cells is properly illustrated in Figure 1. Aspects of performance, noise tolerance and robustness to radiation effects were observed.

The purpose of the work is to demonstrate the differences between the nominal characteristics of each cell topology. As well as stability aspects, related to static noise tolerance and sensitivity to radiation effects. Another important factor is to warn about the impacts related to negligence of this parameter during the characterization of SRAM cells. The analyses aim to contribute by showing the advantages and disadvantages of using a certain topology in view of the specific requirements of the project.

II. Methodology

The development of this work is divided into three steps: The evaluation of power and timing; The study of stability through noise margins; The analysis of the radiation effects. The experiments were performed through electrical simulations, using NGSPICE tool. A high performance (HP) predictive model was used in the 16nm CMOS technology [13]. This model operates with a supply voltage of 0.7V.

A 256-bit architecture of memory was built, in block format. The architecture has two columns of 128 cells each. Connected the columns are the auxiliary circuits, writing, pre-charge, signal amplifier and line/column decoders. This structure covers all the main features found in a real architecture.

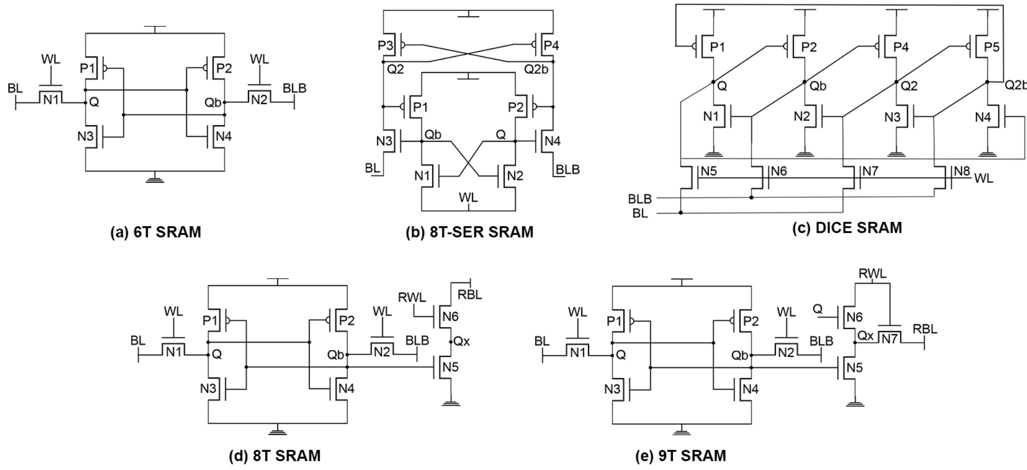

Fig. 1. Electrical diagram of cells

Each cell topology was introduced to the architecture respecting the peculiarities of its design. The memories had a specific sizing following the conventions found in the literature [11]. Cell 6T was implemented with a β-ratio of 1.45x, where: the W of transistors P1-P2-N1-N2 = 32nm and N3-N4 = 45nm. Cells 8T and 9T and DICE were designed with a minimum β-ratio: the W of transistors P1-P2-N1-N2-N3-N4 = 32nm and N5-N6-N7 = 64nm (N7 only in 9T). In cell 8T-SER, the sizing used was: the W of transistors P1-P2-P3-P4 = 40nm, N3-N4 = 45nm and N1-N2 = 50nm.

A key parameters related to SRAMs are time delays and power dissipated by cells. These characteristics were measured through the delay times and the total current consumed by the system. The delay time of the write operation is measured through the interval between 50% percent of the rising voltage of the wordline signal and 50% percent of the rising voltage of the cell node that is receiving the writing of the logic value. The read operation delay is obtained by the interval between 50% of the rising voltage of the wordline signal and the time that a voltage difference of 35mV between the bitlines is created. To obtain the individual consumption of each cell, a dedicated voltage source was used for the selected cell. By subjecting each cell topology to the same operating cycle, it is possible to measure the current consumed by each cell. In order to calculate these results optimally, a python script was developed.As an output, the simulator returns the internal voltage of the selected nodes at each instant of time and the current consumed by the selected cell during the simulation. The script reads these output files and calculates the cell delays and consumption. Both stability and robustness are crucial factors in SRAM cells, both characteristics are determined by the cells ability to retain stored data in the presence of adverse factors. In this work, noise tolerance was obtained through the static noise margins, using the graphical method of overlapping tension curves or ”butterfly curves” [14]. The process consists of inserting a voltage source connected to one of the cell storage nodes. A static simulation (DC) is performed, varying the voltage of the source from 0 to the supply voltage of the circuit.

Through these data the butterfly curves are plotted and the side of the largest internal square the curves are found. The static noise margins during hold (HSNM), during read (RSNM) and during write (WSNM) were evaluated. This technique is very popular due to its easy automation via electrical simulation. To perform the experiments related to the effects of radiation, an analytical model was used that associates the effects of the collision of the radiation particle with a current pulse [15]. The simulation of this pulse is performed by inserting a current source connected to one of the sensitive nodes of the cell.For each sensitive node, scenarios 010 and 101 were evaluated.

The experiment consists of writing a logical value in the cell. This value is associated with the target test scenario. After the writing, the cell remains in hold and then the failure is then injected into the sensitive nodes. After the insertion, the storage value in the cell is checked a few moments later.Thus, checking whether or not there was inversion in the stored data. In a positive case to bitflip, the current value associated to the pulse is reduced. In a negative case, the value is increased. This process was repeated successively, applying a search algorithm to adjust the intensity of the pulse and find the critical load or minimum load causing the bitflip. This process was also automated, the script runs the simulation for each sensitive node, looking for the lowest critical load capable of affecting the cell. The interactions occur using a range of Linear Energy Transfer (LET - MeV.cm²/mg) found on the Earth's surface, that is, up to 40 LET [16].

III. Power and Delay Evaluation

The read and write timing, and the energy consumption results are available in Table I. the 6T SRAM cell needs for longer period to carry out the write operation in comparison with the read. The write operation performed about 7x times longer than the read. So, its defines the write operation as the critical delay of the 6T cell. This result can be explained,

basically, due to the cell ratio. The increase of the β-ratio improves significantly the stability of the cell and facilitates the read operation, in contrast it increases the power consumption, the occupied area and worsens the write delay.

The 8T ans 9T cells are very similar in terms of topology, and this was reflected in their delay times. As in the 6T SRAM, the write delay was greater in relation to the read. However, write occurred only 3x more slowly than read. This is again due to the size of the cells. Both 8T and 9T cells are composed of a dedicated read mechanism. This mechanism allows these cells to operate a read without the need to access their internal storage nodes. Through this characteristic it is possible to decrease the β-ratio to 1 without compromising the functional state of the SRAM.The 6T cell showed a power consumption around 23% higher than the consumption of 8T cell. The 8T cell showed the lowest consumption among all the others cells evaluated in this study. This consumption was very similar to that of 9T cell, which was only about 5% higher. An important characteristic, illustrated by these results, is the fact that 8T and 9T cells had a lower consumption. This fact is even more evident because both cell have a greater number of transistors compared to 6T. As 8T and 9T cells have a minimum β-ratio, increasing the voltage of the storage nodes is easier. Therefore, the PMOS transistor of the complementary inverter stops to conduct quickly. Thus, the peak consumption characterized by the time that the internal transistors conduct simultaneously is reduced. In addition, isolation during the read operation keeps storage nodes disconnected from bitlines. There is no need for energy expenditure to maintain the stability of the stored data after connection with the bitlines.

The 8TSER cell had a 2x longer delay in performing the write operation than in relation to the read operation. However, this cell has a very peculiar structure in comparison to the others cells evaluated in this work. Mainly due to operating with the grounded pre-charge. The fact is that, since the 8TSER pass transistors are of the NMOS type and the bitlines are pre-charged in ground. Increasing the voltage of the bitlines from the cell it becomes a very costly process. This work adopted a difference of 0.35mV of voltage between the bitlines, as a parameter for measuring the read delay. Others approaches use a 0.70mV, for example. It was observed that when working with small increases in these voltage differences, the impact on the read delay grows dramatically, differently from the other topologies. The 8TSER cell obtained the highest consumption. The consumption values of this cell exceeded by more than 3x the consumption compared to 8T cell.

TABLE I
TIME AND POWER CONSUMPTION RESULTS

SRAM Cell	Time Results		Consumption Results	
	Write (ps)	*Read (ps)*	*Energy (fJ)*	*Power (nW)*
6T	14.00	1.99	1.35	117.86
8T	11.99	7.99	1.10	96.16
9T	11.99	7.99	1.16	101.95
8TSER	12.00	6.00	3.69	323.16
DICE	15.99	2.00	2.78	243.44

The DICE cell showed the greatest discrepancy between read and write delays. Write occurred about 8x more slowly than read operation. This cell has a behavior very close to that 6T in several factors. However, due to the redundancy mechanisms existing in this cell, it was possible to apply a minimum sizing to all the transistors without affecting their functionality. This, in theory, would positively affect the write delay and negatively the read delay. What is not reflected in the results presented. The explanation for this is related to the process of write and read operations. In write, it is necessary to raise/lower the voltage of the storage nodes simultaneously with the voltage of the redundant nodes. All of this through the same bitlines, that is, a process that takes more time. In read operation process, the behavior is opposite. There are two nodes lowering the voltage of the bitline to create the voltage difference, facilitating the process.

The DICE cell is just behind the 8TSER cell, with a power consumption about 2.5x grater than consumption compared to 8T. The power consumption of the DICE cell is associated with a longer period of simultaneous conduction of the internal transistors. Now the high consumption of the 8TSER cell it is related to simultaneous conduct, but mainly due to the characteristics of its architecture. As it operates with a pre-charge in ground, the effort to raise the voltage of the bitlines directly impacts the cells total consumption. Another fact to note is that considering the general consumption within the architecture, the grounded pre-carge does not present energy expenditure.

IV. Static Noise Margins Results

The results of the experiments related to data integrity in the presence of static noise are illustrated in Table II. The results are arranged in three categories: Hold static noise margins (HSNM); Read static noise margins (RSNM); Write static noise margins (WSNM).

The experiments showed that all cells demonstrate the same levels of noise tolerance while operating in hold mode. The writing operation presented a greater robustness to the noise in relation to hold state. On average, the cells showed a 50% greater tolerance during write operation, with the exception of the 8TSER cell witch showed a 2x greater tolerance. This result is expected since the voltage at the storage nodes is being guaranteed by the write circuit throughout the operation.

The read operation is considered a critical point in the context of static noise margins. Both 6T and DICE cells showed worrying noise margins during read. The values were about 3x lower than the average of hold cells. These results can be explained by the fact that both cells do not have mechanisms that isolate or guarantee the data contained in the stored nodes.

V. Radiation robustness Evaluation

The results of robustness to the radiation effects are available in Table III. This work developed experiments using a range of LET up to 40 MeVcm²/mg, since its objective is

TABLE II
NOISE MARGINS RESULTS (MV)

SRAM	HSNM	RSNM	WSNM
6T	179.09	53.33	280.70
8T	180.87	180.87	291.90
9T	180.87	180.87	291.90
8TSER	180.85	180.85	359.10
DICE	179.09	53.33	280.70

TABLE III
LET THRESHOLD RESULTS (MEV CM^2/MG)

SRAM Cell	010				101			
	Q	*Qb*	*Q2*	*Q2b*	*Q*	*Qb*	*Q2*	*Q2b*
6T	0.26	0.26	——-	——-	0.10	0.10	——-	——-
8T	0.18	0.18	——-	——-	0.09	0.09	——-	——-
9T	0.18	0.18	——-	——-	0.09	0.09	——-	——-
8TSER	0.28	0.28	40.00	40.00	40.00	40.00	0.14	0.14
DICE	17.23	17.23	10.19	17.23	40.00	40.00	40.00	40.00

to consider terrestrial interactions. The cell nodes that reached this value without bitflip were considered robust in the context of the simulation environment.

The initial experiments found the sensitive nodes of the cell. 6T, 8T and 9T cells have two sensitive nodes, Q and Qb. The 8TSER and DICE cells have four sensitive nodes Q, Q2, Qb and Q2b. The fact that a cell has twice as many sensitive nodes, directly impacts a greater probability of a particle strike with to critical region. However, both 8TSER and DICE cells showed total immunity to the effects of radiation in half of the test cases. The 8TSER cell implement a isolation mechanism in storage nodes, which varies depending on the stored data. The DICE cell uses a redundancy system between its nodes, feeding back the storage data.

Considering the cases in which it does not hear total tolerance, the DICE cell showed the highest LETth values. Then the 8TSER cell which obtained much lower results in relation to DICE. 6T cell was more robust than 8T and 9T cells, showing the influence of sizing also on the characteristics of robustness to radiation.

VI. CONCLUSION

This work demonstrated the impact of radiation effects on the design and construction of SRAMs in nanotechnology. All cells evaluated were implemented and had their structure duly validated.The main characteristics related to the reliability of SRAMs were presented, with the measurement of delay times, energy consumption, noise tolerance and radiation robustness.

The 6T and DICE cells obtained the best reading delay, but presented a worrying result for RSNM, being this the main negative point of both. In the case of the DICE cell, as negative points, we have the high energy consumption and the largest area occupied among the evaluated cells. However, this cell showed the greatest robustness to the radiation effects, presenting a relatively larger LETth in practically all test cases. The 8T, 9T cells obtained the best writing delay as well as the best energy consumption result, being 8T the best in this factor. Both cells obtained good results for the noise margins. As a negative point, we have its higher number of transistors in relation to 6T. 9T obtained similar results to 8T but did not have the best result in any of the characteristics evaluated. Cell 8TSER obtained the best results in SNM. The cell obtained values equivalent to 8T and 9T for HSNM and RSNM, entertaining had a better performance in WSNM. It also obtained considerable advances when the radiation robustness, in relation to cell 6T, 8T and 9T. The main negative points of this topology were the high energy consumption that the cell presented. The 8TSER and DICE cells demonstrated immunity in half of the simulations performed.

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